TQ-Minimodul

TQM167U

mit

Microcontroller SAB-C167

Hardware - Manual

Hardware Manual for:

TQM167U	Rev100
	Rev102
	Rev103
	Rev104
	Rev105
	Rev106
	Rev107
	Rev108

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1 Introduction

TQ embedded Microcontroller Systems

High integration and high reliability are what set the TQ-Components industrial microcontroller modules apart from the rest. TQ-Components Minimodules from credit-card to half credit-card size are unbeatable in various applications. With an ever-expanding product line and clear technology migration path, TQ-Components offers OEMs uncompromising excellence in microcontroller modules. In a variety of industrial measurement, process regulation and control developments engineers confronted with the task of developing a complex monitoring / control system under time constraints are the prime beneficiaries of our microcontroller devices. Compare the advantage of the implementing a TQ-Components module to the total cost of a completely new circuitry design.

Time to market

TQ-Components microcontroller modules provide a drop-in CPU solution, with complete CPU kernel functionality on board. This enables engineers to take a project from concept to prototype or market in weeks, rather than in months or longer.

Reliability

TQ-Components modular embedded microcontroller Minimodules have proven to be reliable and rugged in numerous demanding and critical applications. Our highly knowledgeable team of electronic engineers has wide experience in designing embedded microcontroller Modules. The team‘s commitment to quality and reliability is evident throughout the whole TQ-Components product line.

Upgradability

Thanks to the flexibility of TQ’s product architectures, you will be able to enhance your products by taking advantage of a new technology as when it becomes available. Our products offer a migration path so you can upgrade features or performance without major redesign.

TQ-Minimodules offers you ...

☑ **Best price-performance relationship**

- uncompromising use of most modern production-technology
- low price through high production quantity
- Customised Versions on requests

☑ **Maximum performance on small footprint**

- double-sided SMT Technology
- Fine Pitch Multilayer Printed Circuit Boards
- using latest chip technology
- using latest Flash Memory technology

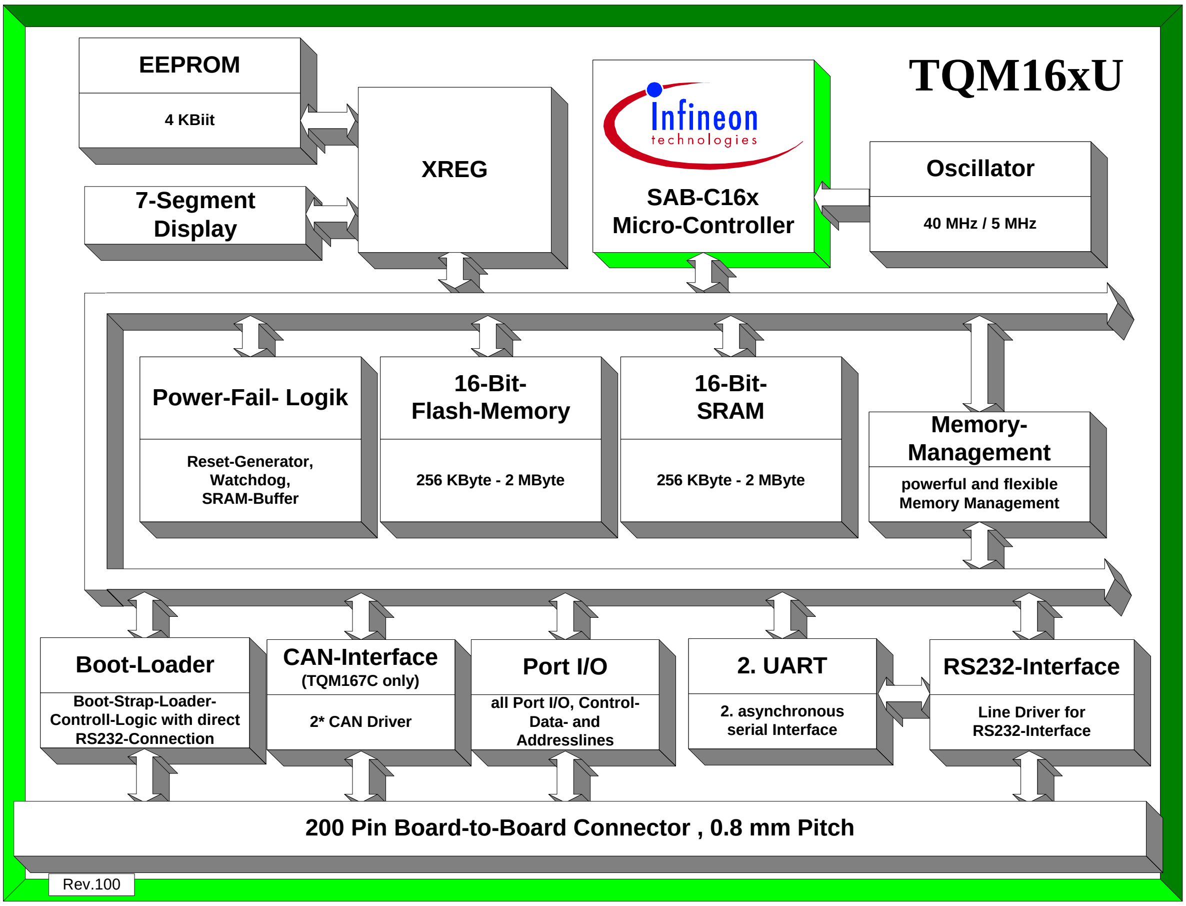
☑ **save time and money in your development**

- complete CPU kernel functionality on board
- immediate start through particular monitor-program
- works with most modern Software Development Tools such as compilers and debuggers
- Design-In Support through the manufacturer

☑ **save time and money in your production and service**

- Download-Function for development, production and service
- simple Firmware-Updates through Download-Function
- Download over Standard RS232-Interface without additional switches and jumpers

2 Block-Diagram



2.1 Microcontroller SAB-C167CR-LM / SAB-C167CS-32FM

- High Performance 16 Bit-CPU
- 100 ns Instruction Cycle Time at 20 MHz CPU
- Up to 16 MByte Linear Address Space for Code and Data
- On-Chip CAN Interface (Version 2.0B) (1x SAB-C167CR-LM / 2x SAB-C167CS-32FM)
- 16-channel 10-bit A/D Converter
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with five 16-bit Timers
- Programmable Watchdog Timer
- Two Serial Channels (Synchronous/Asynchronous and High-Speed Synchronous)
- On-Chip Bootstrap Loader

Details see Siemens / Infineon User's Manual SAB-C167

2.2 Memory

2.2.1 Flash-Memory

- 256 kByte to 2 MByte
- organisation, 128k*16, 256k*16 or 512k*16, 1M*16,
- 90 or 70 ns access time
- on Board programmable
- Standard: 1 MByte

2.2.2 SRAM-Memory

- 256 kByte to 2MByte
- organisation 2*128k*8, 2*512k*8, 2*1M*8,
- 55 ns access time
- external battery backup
- Standard: 256 kByte

2.2.3 Serials EEPROM

- 4 kBit
- organisation 512 * 8 Bit
- EEPROM is handled from XREG

2.3 Reset-Logic

- CPU internal Watchdog
- Power-Fail Logic with MAX808

2.4 Interface

2.4.1 Serial-Interface

- one internal asynchronous (integrated in the processor)
  - used unbuffered as RxD0 and TxD0
  - with RS232 Driver as RxD0# and TxD0#
- one internal synchronous (integrated in the processor)
- one external asynchronous (ST16C550)

2.4.2 CAN-Interface

- two internal CAN-Interfaces (integrated in the processor)

2.4.3 Bus-Interface

- Port I/O, Control- Data- and Addresslines
- No Bus Drivers

2.4.4 Internal Bootstrap Loader

- Download via serial Interface
- Powerful Download Tools
- Download to SRAM or Flash

2.5 XREG

External 16Bit Register to handle 7 Segment Display and EEPROM

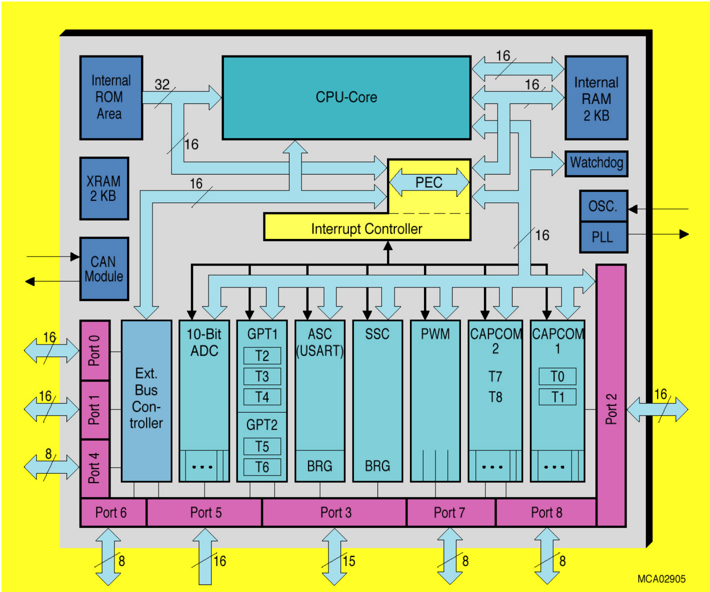
2.6 7Segment Display

- Free programmable Display (handled from XREG.
- Green display colour for standard module types.

2.7 Internal LED

The LED installed on the top of the module is connected to the reset output RSOUT# of the module. It lights when RSOUT# is active, i.e. until the EINIT command has been executed after a reset.

3 Microcontroller



- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- Enhanced Boolean Bit Manipu-lation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Clock Generation via on-chip PLL or via direct clock-input
- Up to 16 MBytes Linear Address Space for Code and Data
- 4/11 KBytes On-Chip SRAM (2/3 KB Internal RAM, 2/8 KBytes Extension RAM) (167CR/167CS)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-bit or 16-bit External Data Bus
- Five Programmable Chip-Select Signals
- Hold- and Hold-Acknowledge Bus Arbitration Support
- 1024 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40 ns
- 16/24-Channel 10-bit A/D Converter with 9.7/7.8 µs Conversion Time (167CR/167CS)
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with five 16-bit Timers
- Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- On-Chip CAN Interface 2.0 B active with 15 Message Objects (Full-CAN/Basic-CAN) (1* at SAB-C167CR / 2* at SAB-C167CS)

- Programmable Watchdog Timer
- Up to 111 General Purpose IO Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader

Details see Siemens / Infineon User's Manual SAB-C167CR / SAB-C167CS

4 Memory

The flexible memory management of the TQM167U is different to most microcontroller modules of the same generation. The handling of the configuration of this module is more simple and flexible than in almost any other module.

The installed processor is equipped with 5 freely programmable Chip Select outputs which access the respective system components. This allows a completely open memory configuration of the Minimodule.

The memory management is described in detail in ➩ Section4.4.

4.1 Flash-Memory

4.1.1 Flash-Memory structure

Depending on the module variant, the non-volatile memory of the module is implemented with one 16-bit flash EPROM with variable storage capacity. This results in a possible memory space of 128K*16, 256k*16, 512K*16 or 1M*16 representing as memory capacity of 256 kByte, 512 kByte, 1 MByte or 2 Mbyte. The module TQM167U is therefore available with a maximum non-volatile memory of 2 MByte.

For exact technical data of the applied memory chips, please refer to ➩ Section 10.

Details on programming are to be found in ➩ Section 4.1.2 / 4.3.6

Depending on the equipping, the following memory configurations are possible:

Flash1	Capacity:	Address space:
256 kByte	256 kByte	128k x 16
512 kByte	512 kByte	256k x 16
1 MByte	1 MByte	512K x 16
2 Mbyte	2 Mbyte	1 M x 16

4.1.2 Flash EPROM BUSCON

The BUSCON is dependent from the memory access time, type of Module (multiplexed or demultiplexed data bus mode) and latched or unlatched programmed Chip Selects.

In strict compliance with the specifications, the following configurations are therefore possible:

BUSCON 0		
	CS - Mode	
Bus type	**Latched** **CSCFG = 0**	**unlatched** **CSCFG = 1**
70ns demultiplexed	**04BEh** (1 WS) 150ns	**04BEh** (0 WS) 100ns
90ns demultiplexed	**04BEh** (1 WS) 150ns	**04BEh** (1 WS) 150ns
70ns multiplexed	**04EEh** (1 WS) 200ns	**04EFh** (0 WS) 150ns
90ns multiplexed	**04EEh** (1 WS) 200ns	**04EEh** (1 WS) 200ns

☞ *Example: (70ns Flash EPROM, Multiplexed Bus, CSCFG =1)*

Field in BUSCON:	Value:	Delay:
MCTC [BUSCON 0.0...3]	1111b	0 Waitstate
RWDC [BUSCON 0.4]	0b	
MTTC [BUSCON 0.5]	1b	No Delay

The associated C command could then be as follows:

➔ BUSCONx = 04EFh

4.2 SRAM-Memory

4.2.1 SRAM-Memory structure

The static memory of the module is implemented by two 8-bit SRAMs with memory space of max 1M*16, representing a memory capacity of 2 MByte. The SRAM can be protected against data loss by a battery buffer. The associated connections are provided on the module.

For exact technical data of the applied memory chips, please refer to ➩ Section 10.

Details on programming are to be found in ➩ Section 4.2.2 / 4.3.7

Depending on the installed chips, the following memory configurations are possible:

SRAM1	SRAM2	Capacity:	Address space:
128 KByte	128 KByte	256 KByte	128K x 16
512 KByte	512 KByte	1MByte	512K x 16
1MByte	1MByte	2MByte	1M x 16

* Due to the 16-bit data and address buses, both memory chips are always installed *

4.2.2 SRAM access times

The static RAMs installed in the modules have a maximum access time of 55ns. The access speed can be programmed by the fields MCTC (Memory Cycle Time Control), MTTC (Memory Tri-State Time Control) and RWDC (Read/Write Delay Control) of the respective BUSCON register.
The BUSCON is dependent from the memory access time, multiplexed or demultiplexed Data bus mode and latched or unlatched programmed Chip Selects.

In strict compliance with the specifications, the following configuration is therefore possible:

BUSCON 1		
	CS - Mode	
Bus type	**Latched** **CSCFG = 0**	**unlatched** **CSCFG = 1**
55ns demultiplexed	**04BEh** (1 WS) 150ns	**04BFh** (0 WS) 100ns
55ns multiplexed	**04EEh** (1 WS) 200ns	**04EFh** (0 WS) 150ns

☞ *Example: (55ns SRAM memory, demultiplexed Bus, CSCFG =0)*

Field in BUSCON:	Value:	Delay:
MCTC [BUSCON 0.0...3]	1110b	1 Waitstate
RWDC [BUSCON 0.4]	1b	
MTTC [BUSCON 0.5]	1b	No Delay

The associated C command could then be as follows:

➔ BUSCONx = 04BEh

4.3 SerialsEEPROM

The EEPROM is switchable and work in a 8bit or 16bit modus.

Details on programming are to be found in ➪ Section 4.4.5.2

4.4 Memory Management

This section contains all details and the know-how necessary for optimum usage of the memory installed in the module. The memory range management and configuration (memory management) can be implemented entirely by software. The address ranges can be programmed flexibly with the 5 freely programmable CS outputs of the processor and the associated configuration registers.

4.4.1 Principle of operation

The microcontroller SAB-C167CR/CS is equipped with 5 freely programmable Chip Select outputs which allow access to the respective periphery. For each address block allocated to a Chip Select output, it is also possible to select an individual configuration of the system bus. For this, the bus type, bus width, wait states and also the memory block can be allocated to a CS signal.

CS0 addresses all memory blocks of the addressable range not allocated to CS1-CS4. This makes it possible to manage non-sequential memory blocks without further measures. After a reset, the Chip Select lines CS1-CS4 of the processor are inactive. In this case, CS0 is active for the entire memory range.

To allow programs in the flash EPROM to be started, CS0 is used to address these memory chips after a reset.

4.4.2 Chip Select allocation

The memory configuration applicable in most cases is works-adjusted by the manufacturer:

- CS0 addresses the flash EPROMs,
- CS1 the SRAMs.

For programming, please refer to ➪ Section 4.4.4 of this description.

Standard settings by TQ-Components:

Control line	Connected chip		
CS0#	On-board flash EPROM		
CS1#	On-board SRAM		
CS2#	external. UART / XREG		
CS3#	external CS-Signal		
CS4#	external CS-Signal		
CS0#	Reset configuration	000000_h- $FFFFFF_h$	Flash EPROM

4.4.3 Programming of the Chip Select lines

The Chip Select lines are programmed by software via the registers BUSCON0..4 and ADDRSEL1..4.

The BUSCON registers define the hardware configuration of the system bus, the ADDRSEL registers the scope and size of memory.

In this, it must be observed that ADDRSEL0 does not exist because, as described in Sect. xx, all memory space outside the defined ranges of CS1-CS4 is allocated to the Chip Select line CS0.

BUSCON registers

The BUSCON registers are all adjustable by software. These are not preset apart from the BUSCON0 register.

The following parameter can be set individually through the BUSCON registers for each memory block initialised with the respective CS lines:

- Bus width:
  The system bus can be selected with a width of 8 or 16 bits. If an 8-bit bus is selected, first the Low byte and then the High byte are transferred through the data lines D0-D7.
- Bus type:
  This allows the selection of a multiplexed or non-multiplexed bus.
- Wait states:
  Up to 15 wait states, memory tristates and a R/W delay can be specified.
- Miscellaneous:
  The length of the ALE signal and the functions of RD# and WR# can also be influenced here.

The exact programming is to be found in the Microprocessor manual.

ADDRSEL registers

The division of the memory range is performed with the ADDRSEL registers. For this, the starting address of the memory block and the memory size must be specified:

ADDRSELx:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Range Start Address												Range Size Selection			

- **Range Start Address (RGSAD)**
  specifies the starting address of the memory block for the respective CS line (only integer multiples of the adjusted block size (RGSZ) are valid as the starting address; see table).

- **Range Size Selection (RGSZ)**
  Specifies the memory size as shown in the table below.

The following table is intended to simplify programming.

RGSZ:	Memorysize	RGSAD:	Startaddress
0 0 0 0	4 Kbyte	$RRRRRRRRRRRR_b$	$RRRRRRRRRRRR_b$ * 4KByte
0 0 0 1	8 Kbyte	$RRRRRRRRRRRx_b$	$RRRRRRRRRRR0_b$ * 4KByte
0 0 1 0	16 Kbyte	$RRRRRRRRRRxx_b$	$RRRRRRRRRR00_b$ * 4KByte
0 0 1 1	32 Kbyte	$RRRRRRRRRxxx_b$	$RRRRRRRRR000_b$ * 4KByte
0 1 0 0	64 Kbyte	$RRRRRRRRxxxx_b$	$RRRRRRRR0000_b$ * 4KByte
0 1 0 1	128 Kbyte	$RRRRRRRxxxxx_b$	$RRRRRRR00000_b$ * 4KByte
0 1 1 0	256 Kbyte	$RRRRRRxxxxxx_b$	$RRRRRR000000_b$ * 4KByte
0 1 1 1	512 Kbyte	$RRRRRxxxxxxx_b$	$RRRRR0000000_b$ * 4KByte
1 0 0 0	1 MByte	$RRRRxxxxxxxx_b$	$RRRR00000000_b$ * 4KByte
1 0 0 1	2 MByte	$RRRxxxxxxxxx_b$	$RRR000000000_b$ * 4KByte
1 0 1 0	4 MByte	$RRxxxxxxxxxx_b$	$RR0000000000_b$ * 4KByte
1 0 1 1	8 MByte	$Rxxxxxxxxxxx_b$	$R00000000000_b$ * 4KByte
Rest:	Not defined		

R: used bit; x: unused bit

☞ *Example:*

ADDRSEL4 = 1A42h; (= 0001 1010 0100 0010_b)

Specifies a 16 KByte block of memory from address $1A4000_h$ for access to external memory.

4.4.4 Programming the SYSCON registers

The TQM167U takes the Byte access to the 16 Bit Bus with the Signals WRL# and WRH#.
WRL# will be active, when you write to the lowest Byte (LBS).
Therefore Bit **WRCFG** in the SYSCON will be setted.

➔ WRCFG = 1
➔

The SAB-C167 can use the Chip Select Signals on two different Modes.

4.4.4.1 Latched CS# Modus

After the ALE Signal lost his value the CS# - Signals change his level.
Therefore this Modus shows a clear but a slow Bustiming.

4.4.4.2 Unlatched CS# Modus

The CS# -Signals changing together with the Addresslines his level. The Bustiming is fast. Therefore it could be that we have on the CS# lines some Spikes between the bus access times. The Spikes takes no effect on theTQM167U. Please be careful with your on Peripheries.

Details see Siemens / Infineon User's Manual SAB-C167CR / SAB-C167CS

4.4.5 Programming the XREG/External UART

BUSCON2 will be configured as a 8-Bit –Bus with RW/Delay and an minimum of 2 Waitstates.
➔ BUSCON2 = 060Dh

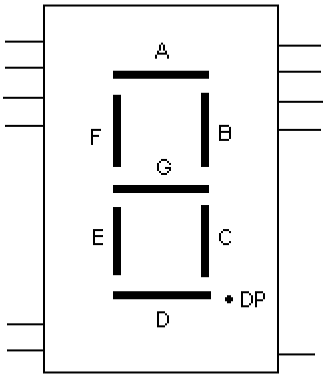
4.4.5.1 Address Area from the XREG

The XREG is addressed when A10 = 1, A11 = 0 and CS#2 = 0.
Because of that it results a relative Address area from 0400h – 07FFh.
Only the Addresses 400h and 401h are used.

4.4.5.2 Configuration from the XREG

Relative Address 400h

Bit	7	6	5	4	3	2	1	0
Meaning	DP	G	F	E	D	C	B	A
Read/Write	W	W	W	W	W	W	W	W
Function	7 – Segment - Display							



Relative Address 401h

Bit	7	6	5	4	3	2	1	0
Meaning	DNU	DNU	XR13	XR12	ORG	STRB	CLR	Data
Read/Write	W	W	W	W	W	W	W	R/W
Function	Free for Ex		Port Pins		EEPROM 93C66			

W: only Write
R/W: Read and Write
DNU: Do not use / set to 0

4.4.5.3 Address Area UART

The UART is addressed when A11 = 1 and .CS#2 = 0
Because of that it results a relative Address area from 0800h – 0FFFh.
Only the Address area from 800h - 807h is used.

4.4.5.4 Free Address Area from CS 2#

A free relative Address Area on CS2# from 0000h – 03FFh can be used for external Applications.

4.4.6 Programming the flash EPROMs

Bit A0 of the flash EPROM is connected to A1 of the address bus. Therefor the Flash EPROM an be programmed only wordwise. During programming the addresses which are used has to be doubled.

If the Flash EPROM should be programmed bytewise following procedure should be used:

1. Read out the data word which has the byte that should be changed
2. Change the byte
3. Write back the data word.

☞ *Example:* Word Program

	1st Buscycle		2nd Buscycle		3rd Buscycle		4th Buscycle	
	Addresss	Data	Address	Data	Address	Data	Address	Data
Standard	5555h	00AAh	2AAAh	0055h	5555h	00A0h	PA	Data
TQM167	AAAAh	00AAh	5554h	0055h	AAAAH	00A0h	PA	Data

PA: the address to be programmed is equal in both cases.

4.4.7 Examples of memory configurations

The Examples are configured with 70ns FLASH and demultiplexed BUS

4.4.7.1 Memory allocation used by the monitor Program MON16U and C166Mon (Keil)

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-1FFFFFh	SRAM	1	04BFh	0009h
200000h-3FFFFFh	Flash-EPROM	0	04BFh	--------
400000h-400FFFh	External Uart / XREG	2	060Dh	4000h
500000h-5FFFFFh	External Memory	3	048Eh	5008h

4.4.7.2 Memory allocation after download to the RAM

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-1FFFFFh	SRAM	1	04BFh	0009h
200000h-3FFFFFh	Flash-EPROM	0	04BFh	--------

These are two concrete proposals of memory configurations which ensure stable operation:

Variant for a program in flash memory
Variant for a program in SRAM

5 Interface

5.1 Serial Interface

The module is equipped with three serial interfaces:

- one internal asynchronous (integrated in the processor)
- one internal synchronous (integrated in the processor)
- one external asynchronous (ST16C550)

5.1.1 Internal asynchronous interface

Initialisation:

The internal asynchronous interface operates directly with the processor clock. For programming, please refer to the initialisation recommended in the manual.

Hardware configuration:

The interface is equipped with two connections on the module:

- Unbuffered as RxD0 and TxD0.
- With RS232 driver as RxD0# and TxD0#.

5.1.2 Internal synchronous interface

Initialisation:

See ⇨ Section 5.1.1

Hardware configuration:

The conductors of the synchronous interface are connected to port 3 and can be used without limitations. This Interface can be used up to 5 Mbaud.

P3.8 MRST

P3.9 MTSR

P3.13 SCLK

5.1.3 External asynchronous interface

Initialisation:
The external asynchronous interface operates directly with the 16C550.
The UART interface is accessed at Chip Select 2 (CS2#)
The frequency of XTAL1/2 is 14,7456 MHz
INT is connected over 1 K to pin P7.6 from the C167.

Hardware configuration:
The interface is equipped with two connections on the module:

- Unbuffered as RxD1 and TxD1.
- With RS232 driver as RxD1# and TxD1#.

5.2 CAN - Interface

- Unbuffered as CAN1-RxD and CAN1-TxD and CAN2-RxD and CAN2-TxD.
- With CAN driver (2 X PCA82C251) as CAN1_H and CAN1_L and CAN2_H and CAN2.

5.3 Bus - Interface

All Port I/O, Control- Data- and Addresslines are available and connected to X1 and X2.

For Pin Configuratin, please refer to ⇨ Section 6 of this description.

5.4 Internal bootstrap loader

The installed processor is equipped with a bootstrap loader which, in conjunction with the periphery implemented in the module, makes programming of the EPROMs unnecessary.

The downloading of a program to the module can be performed via the serial interface

In this way, programs can be downloaded from a PC without additional hardware, either to the SRAM or to the flash EPROM.

Because the internal bootstrap loader of the processor can only process 32 bytes, it is necessary to transfer programs in several blocks into the memory of the module.

Functional sequence:

1. To activate the bootstrap loader, a reset must first be initiated (RTS and DTR active = 1).
2. The reset is enabled after approx. 10 ms, the DTR line remains active.
3. The processor then enters the bootstrap loader mode and waits for a Null byte transmitted via ASC0.
4. The processor then returns an acknowledgement byte ($A5), which can be used to identify the processor.
5. 32 bytes are then transmitted by the PC, which are loaded directly into the internal RAM of the processor.

To allow convenient downloading of programs with larger memory requirement, TQ has developed the program BOOT16x (DOS Version) and TQLoad (Windows Version).

The program BOOT16x provides user-friendly control of the entire loading operation.

More detailed explanations and examples of this are to be found in the Software Manual.

The following signal lines of the serial interface are used (by the PC) for the download:

TQM167 Signal	TQM167 Pin		PC (DSUB-9) Pin	PC (DSUB-9) Signal	PC (DSUB-25) Pin	PC (DSUB-25) Signal
RESINS#	X1-52	↔	7	RTS	4	RTS
TXD0#	X1-55	↔	2	RxD	3	RxD
GND	X1-2	↔	5	GND	7	GND
GND	X1-40	↔	5	GND	7	GND
BOOTSTR#	X1-53	↔	4	DTR	20	DTR
RXD0#	X1-56	↔	3	TxD	2	TxD

6 Power supply

6.1 Supply voltage

The supply voltage for the TQM167U is defined as follows:

Vcc = 5V ± 4,5% = 4,775V ..5,225V

The tolerances of supply voltage depend on the used supervisor circuit MAX808L.

6.2 Maximum supply current

The maximum supply current for the TQM167U is defined as follows:

With 7 segment display: I_{max} = 250mA

Without 7 segment display: I_{max} = 200mA

7 Pin Configuration

This chapter describes the function of the TQM167U connections.

7.1 CPU Pins

Signal	CPU-Pin	Module-Pin	Type	Description
P0L.0 / AD0	100	X1-32	I/O	P0L.0 – direct connected buffered
P0L.1 / AD1	101	X1-31	I/O	P0L.1 – direct connected buffered
P0L.2 / AD2	102	X1-30	I/O	P0L.2 – direct connected buffered
P0L.3 / AD3	103	X1-29	I/O	P0L.3 – direct connected buffered
P0L.4 / AD4	104	X1-28	I/O	P0L.4 – direct connected buffered
P0L.5 / AD5	105	X1-27	I/O	P0L.5 – direct connected buffered
P0L.6 / AD6	106	X1-26	I/O	P0L.6 – direct connected buffered
P0L.7 / AD7	107	X1-25	I/O	P0L.7 – direct connected buffered
P0H.0 / AD8	108	X1-24	I/O	P0H.0 – direct connected buffered
P0H.1 / AD9	111	X1-23	I/O	P0H.1 – direct connected buffered
P0H.2 / AD10	112	X1-22	I/O	P0H.2 – direct connected buffered
P0H.3 / AD11	113	X1-21	I/O	P0H.3 – direct connected buffered
P0H.4 / AD12	114	X1-20	I/O	P0H.4 – direct connected buffered
P0H.5 / AD13	115	X1-19	I/O	P0H.5 – direct connected buffered
P0H.6 / AD14	116	X1-18	I/O	P0H.6 – direct connected buffered
P0H.7 / AD15	117	X1-17	I/O	P0H.7 – direct connected buffered
P1L.0 / A0 / AN16	118	X2-19	I/O	P1L.0 - direct connected buffered
P1L.1 / A1 / AN17	119	X2-20	I/O	P1L.1 - direct connected buffered
P1L.2 / A2 / AN18	120	X2-21	I/O	P1L.2 - direct connected buffered
P1L.3 / A3 / AN19	121	X2-22	I/O	P1L.3 - direct connected buffered
P1L.4 / A4 / AN20	122	X2-23	I/O	P1L.4 - direct connected buffered
P1L.5 / A5 / AN21	123	X2-24	I/O	P1L.5 - direct connected buffered
P1L.6 / A6 / AN22	124	X2-25	I/O	P1L.6 - direct connected buffered
P1L.7 / A7 / AN23	125	X2-26	I/O	P1L.7 - direct connected buffered
P1H.0 / A8	128	X2-27	I/O	P1H.0 - direct connected buffered
P1H.1 / A9	129	X2-28	I/O	P1H.1 - direct connected buffered
P1H.2 / A10	130	X2-29	I/O	P1H.2 - direct connected buffered
P1H.3 / A11	131	X2-30	I/O	P1H.3 - direct connected buffered
P1H.4 / A12 / CC24IO	132	X2-31	I/O	P1H.4 - direct connected buffered
P1H.5 / A13 / CC25IO	133	X2-32	I/O	P1H.5 - direct connected buffered
P1H.6 / A14 / CC26IO	134	X2-33	I/O	P1H.6 - direct connected buffered
P1H.7 / A15 / CC27IO	135	X2-34	I/O	P1H.7 - direct connected buffered
P2.0 / CC0IO	47	X2-72	I/O	Port P2.0 – direct connected
P2.1 / CC1IO	48	X2-73	I/O	Port P2.1 – direct connected
P2.2 / CC2IO	49	X2-74	I/O	Port P2.2 – direct connected
P2.3 / CC3IO	50	X2-75	I/O	Port P2.3 – direct connected
P2.4 / CC4IO	51	X2-76	I/O	Port P2.4 – direct connected
P2.5 / CC5IO	52	X2-77	I/O	Port P2.5 – direct connected
P2.6 / CC6IO	53	X2-78	I/O	Port P2.6 – direct connected
P2.7 / CC7IO	54	X2-79	I/O	Port P2.7 – direct connected
P2.8 / CC8IO / EX0IN	57	X2-80	I/O	Port P2.8 – direct connected
P2.9 / CC9IO / EX1IN	58	X2-81	I/O	Port P2.9 – direct connected
P2.10 / CC10IO / EX2IN	59	X2-82	I/O	Port P2.10 – direct connected
P2.11 / CC11IO / EX3IN	60	X2-83	I/O	Port P2.11 – direct connected
P2.12 / CC12IO / EX4IN	61	X2-84	I/O	Port P2.12 – direct connected
P2.13 / CC13IO / EX5IN	62	X2-85	I/O	Port P2.13 – direct connected

Signal	CPU-Pin	Module-Pin	Type	Description
P2.14 / CC14IO / EX6IN	63	X2-86	I/O	Port P2.14 – direct connected
P2.15 / CC15IO / EX7IN / T7IN	64	X2-87	I/O	Port P2.15 – direct connected
P3.0 / T0IN	65	X1-78	I/O	Port P3.0 – direct connected
P3.1 / T6OUT	66	X1-77	I/O	Port P3.1 – direct connected
P3.2 / CAPIN	67	X1-76	I/O	Port P3.2 – direct connected
P3.3 / T3OUT	68	X1-75	I/O	Port P3.3 – direct connected
P3.4 / T3EUD	69	X1-74	I/O	Port P3.4 – direct connected
P3.5 / T4IN	70	X1-73	I/O	Port P3.5 – direct connected
P3.6 / T3IN	73	X1-72	I/O	Port P3.6 – direct connected
P3.7 / T2IN	74	X1-71	I/O	Port P3.7 – direct connected
P3.8 / MRST	75	X1-70	I/O	Port P3.8 – direct connected
P3.9 / MTSR	76	X1-69	I/O	Port P3.9 – direct connected
P3.10 / TxD0	77	X1-68	O	Port P3.10 – direct connected Connected to RS232 driver
P3.11 / RxD0	78	X1-67	I	Port P3.11 – direct connected Connected to RS232 driver
P3.12/WRHB#	79	X1-66	O	WRH# active buffered
P3.13 / SCLK	80	X1-65	O	Port P3.13 – direct connected
P3.15 / CLKOUT / FOUT	81	X1-63	O	Port P3.15 – direct connected
P4.0 / A16	85	X1-47	O	Port P4.0 – direct connected Used as Address Line for 2 MB SRAM/Flash
P4.1 / A17	86	X1-46	O	Port P4.1 – direct connected Used as Address Line for 2 MB SRAM/Flash
P4.2 / A18	87	X1-45	O	Port P4.2 – direct connected Used as Address Line for 2 MB SRAM/Flash
P4.3 / A19	88	X1-44	O	Port P4.3 – direct connected Used as Address Line for 2 MB SRAM/Flash
P4.4 / A20 / CAN2_RxD^{167CS}	89	X1-43	O	Port P4.4 – direct connected Used as Address Line for 2 MB SRAM/Flash Connected to CAN2 Driver$^{Option\ 16}$
P4.5 / A21 / CAN1_RxD^{167CR}	90	X1-42	O	Port P4.5 – direct connected Connected to CAN1 Driver $^{Option\ 8}$
P4.6 / A22 / CAN1_TxD^{167CR}	91	X1-41	O	Port P4.6 – direct connected Connected to CAN1 Driver $^{Option\ 8}$
P4.7 / A23 / CAN2_TxD^{167CS}	92	X1-38	O	Port P4.7 – direct connected Connected to CAN2 Driver $^{Option\ 16}$
P5.0 / AN0	27	X2-101	I	Port P5.0 – direct connected
P5.1 / AN1	28	X2-102	I	Port P5.1 – direct connected
P5.2 / AN2	29	X2-103	I	Port P5.2 – direct connected
P5.3 / AN3	30	X2-104	I	Port P5.3 – direct connected
P5.4 / AN4	31	X2-105	I	Port P5.4 – direct connected
P5.5 / AN5	32	X2-106	I	Port P5.5 – direct connected
P5.6 / AN6	33	X2-107	I	Port P5.6 – direct connected
P5.7 / AN7	34	X2-108	I	Port P5.7 – direct connected
P5.8 / AN8	35	X2-109	I	Port P5.8 – direct connected
P5.9 / AN9	36	X2-110	I	Port P5.9 – direct connected
P5.10 / AN10 / T6EUD	39	X2-111	I	Port P5.10 – direct connected
P5.11 / AN11 / T5EUD	40	X2-112	I	Port P5.11 – direct connected
P5.12 / AN12 / T6IN	41	X2-113	I	Port P5.12 – direct connected

Signal	CPU-Pin	Module-Pin	Type	Description
P5.13 / AN13 / T5IN	42	X2-114	I	Port P5.13 – direct connected
P5.14 / AN14 / T4EUD	43	X2-115	I	Port P5.14 – direct connected
P5.15 / AN15 / T2EUD	44	X2-116	I	Port P5.15 – direct connected
P6.0 / CS1#	1	-	I/O	Port P6.0 – not connected only internal
P6.1 / CS1#	2	-	I/O	Port P6.1 – not connected only internal
P6.2 / CS2#	3	X2-38	I/O	Port P6.2 – direct connected[CS2#] Used as Chip Select line for EEPROM, UART and 7 Segment Display
P6.3 / CS3#	4	X2-39	I/O	Port P6.3 – direct connected
P6.4 / CS4#	5	X2-40	I/O	Port P6.4 – direct connected
P6.5 / HOLD#	6	X2-41	I/O	Port P6.5 – direct connected
P6.6 / HLDA#	7	X2-42	I/O	Port P6.6 – direct connected
P6.7 / BREQ#	8	X2-43	I/O	Port P6.7 – direct connected
P7.0 / POUT0	19	X2-52	I/O	Port P7.0 – direct connected
P7.1 / POUT1	20	X2-53	I/O	Port P7.1 – direct connected
P7.2 / POUT2	21	X2-54	I/O	Port P7.2 – direct connected
P7.3 / POUT3	22	X2-55	I/O	Port P7.3 – direct connected
P7.4 / CC28IO	23	X2-56	I/O	Port P7.4 – direct connected
P7.5 / CC29IO	24	X2-57	I/O	Port P7.5 – direct connected
P7.6 / CC30IO / INT	25	X2-58	I/O	Port P7.6 – direct connected, Interupt line external UART connected via 1kOhm.
P7.7 / CC31IO	26	X2-61	I/O	Port P7.7 – direct connected
P8.0 / CC16IO	9	X2-44	I/O	Port P8.0 – direct connected
P8.1 / CC17IO	10	X2-45	I/O	Port P8.1 – direct connected
P8.2 / CC18IO	11	X2-46	I/O	Port P8.2 – direct connected
P8.3 / CC19IO	12	X2-47	I/O	Port P8.3 – direct connected
P8.4 / CC20IO	13	X2-48	I/O	Port P8.4 – direct connected
P8.5 / CC21IO	14	X2-49	I/O	Port P8.5 – direct connected
P8.6 / CC22IO	15	X2-50	I/O	Port P8.6 – direct connected
P8.7 / CC23IO	16	X2-51	I/O	Port P8.7 – direct connected
NMI#	142	X2-37	I	NMI# - direct connected / int. Connected through 4,7Kohm to VCC
RSTOUT#	141	X2-36	O	RSTOUT# - direct connected / internal Connected to an Inv. (RESET) RST -LED
RSTIN#	140	X2-35	I/O	RSTIN# - direct connected
ALE	98	X1-34	O	ALE - direct connected
EA#	99	X1-33	I	EA# - direct connected / int. Connected through 4,7Kohm to GND
READY#	97	X1-35	I	READY# - direct connected / int. Connected through 4,7Kohm to VCC
RD#	95	X1-37	O	RD# - active buffered
WRLB#	96	X1-36	O	WRLB# - active buffered
V_{PP}	84	X1-50	-	NC
V_{AGND}		X2-118	-	Reference voltage for the A/D converter
V_{AREF}		X2-117		Reference ground for the A/D converter

[167CR] – only for SAB-C167CR
[167CS] – only for SAB-C167CS
[Option 8] – only for CAN Driver 1 / Option 8
[Option 16] – only for CAN Driver 2 / Option 16
[CS2#] - can be not used when Option 2, 4 or 32
= active low or inverted signal

7.2 Module Pins

Signal	Module-Pin	Type	Description
TxD0#	X1-55	O	RS232 output of the internal serial interface ASCO Level adjustment by MAX3232
RxD0#	X1-56	I	RS232 input of the internal serial interface ASCO Level adjustment by MAX3232
TxD1#	X1-57	O	RS232 output of the external serial interface Level adjustment by MAX3232
RxD1#	X1-58	I	RS232 input of the external serial interface Level adjustment by MAX3232
TxD1	X1-14	O	RS232 output of the external serial interface not buffered
RxD1	X1-13	I	RS232 input of the external serial interface not buffered
DTR#	X1-3	O	Data Terminal Ready ST16C550 external UART
RTS#	X1-4	O	Request to Send ST16C550 external UART
OUT1#	X1-5	O	Output 1 (User defined) ST16C550 external UART
OUT2#	X1-6	O	Output 2 (User defined) ST16C550 external UART
RI#	X1-7	I	Ring Indicator ST16C550 external UART
CD#	X1-8	I	Carrier Detect ST16C550 external UART
DSR#	X1-9	I	Data Set Ready ST16C550 external UART
CTS#	X1-10	I	Clear to Send ST16C550 external UART
XR12	X1-16	O	Free programmable XREG output
XR13	X1-15	O	Free programmable XREG output
BAUDOUT#	X1-11	O	Baud Rate Generator output ST16C550 external UART
CAN1_H	X1-60		HIGH level CAN1 voltage input/output
CAN1_L	X1-62		LOW level CAN1 voltage input/output
CAN2_H	X1-59		HIGH level CAN2 voltage input/output
CAN2_L	X1-61		LOW level CAN2 voltage input/output
RSINS#	X1-52		Reset in (Bootstrap Loader)
BOOTSTR#	X1-53		Bootstrap loader input to activate the bootstrap loader mode via the serial interface. Positive voltage bootstrap mode active.
LOWL#	X1-54		Low-Line Comparator output
VBAT	X1-51	-	Backup Battery input
V_{CC} – 5V	X1-1	-	Digital voltage
V_{CC} – 5V	X1-39	-	Digital voltage
V_{CC} – 5V	X1-79	-	Digital voltage
V_{CC} – 5V	X2-1	-	Digital voltage
V_{CC} – 5V	X2-59	-	Digital voltage
V_{CC} – 5V	X2-119	-	Digital voltage
DGND	X1-2	-	Digital ground
DGND	X1-40	-	Digital ground
DGND	X1-80	-	Digital ground
DGND	X2-2	-	Digital ground
DGND	X2-60	-	Digital ground
DGND	X2-120	-	Digital ground

= active low or inverted signal

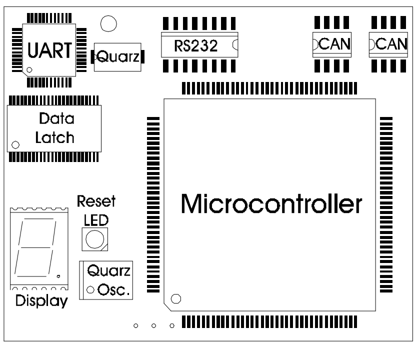
8 Mechanical Data

8.1 Connector

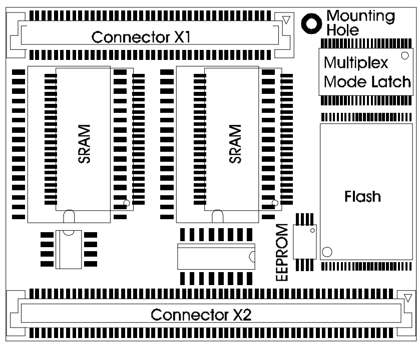
Board-to-Board Distance	Option	Modul			
		No. of Pin	**Qty**	**Supplier**	**Order No.**
5 mm 6 mm 7 mm 8 mm	5	120	1	AMP Berg	177983-5 61082-121000
		80	1	AMP Berg	177983-3 61082-081000

Board-to-Board Distance	Base Board Connector		
	No. Of Pin	**Supplier**	**Order No.**
5 mm	120	AMP	177984-5
		Berg	61083-121000
	80	AMP	177984-3
		Berg	61083-081000
6 mm	120	AMP	5-179029-5
		Berg	61083-122000
	80	AMP	5-179029-3
		Berg	61083-082000
7 mm	120	AMP	5-179030-5
		Berg	61083-123000
	80	AMP	5-179030-3
		Berg	61083-083000
8 mm	120	AMP	5-179031-5
		Berg	61083-124000
	80	AMP	5-179031-3
		Berg	61083-084000

8.2 Connector Position



Top View: TQM167U

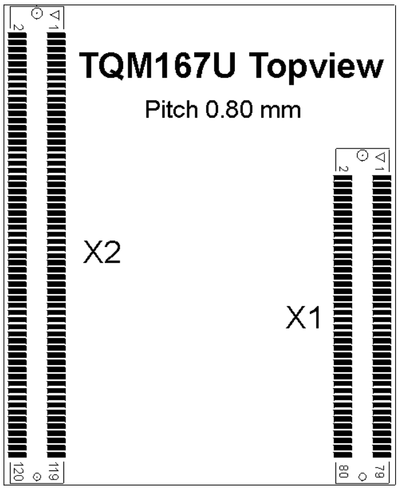


Bottom View: TQM167U

9 Pin Configuration

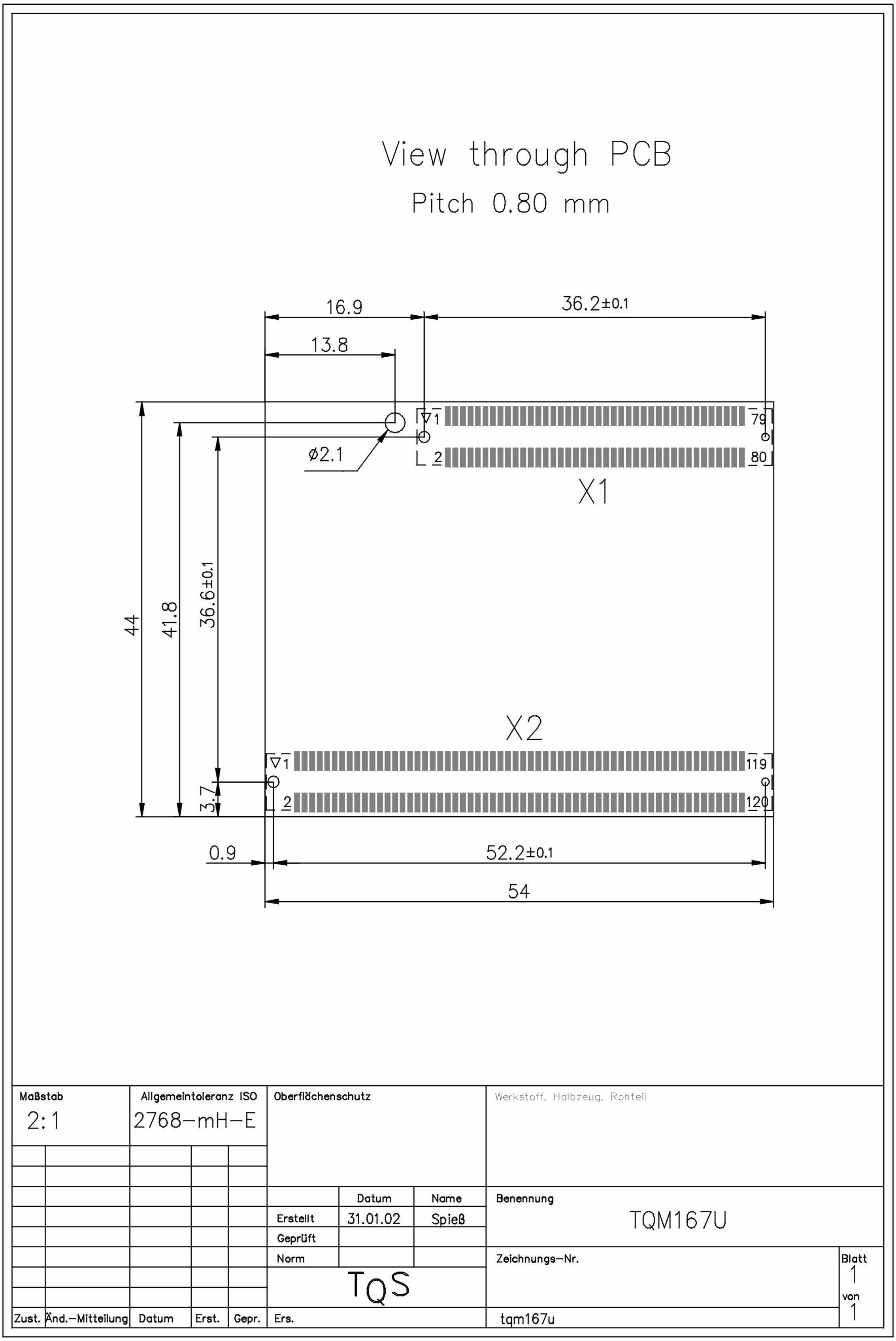
Pin NoX2	Function	Pin NoX2	Function
2	DGND	1	VCC5V
4	*NC – Spare*	3	*NC – Spare*
6	*NC – Spare*	5	*NC – Spare*
8	*NC – Spare*	7	*NC – Spare*
10	*NC – Spare*	9	*NC – Spare*
12	*NC – Spare*	11	*NC – Spare*
14	*NC – Spare*	13	*NC – Spare*
16	*NC - Spare*	15	*NC – Spare*
18	*NC - Spare*	17	*NC – Spare*
20	P1L.1 / A1 / AN17	19	P1L.0 / A0 / AN16
22	P1L.3 / A3 / AN19	21	P1L.2 / A2 / AN18
24	P1L.5 / A5 / AN21	23	P1L.4 / A4 / AN20
26	P1L.7 / A7 / AN23	25	P1L.6 / A6 / AN22
28	P1H.1 / A9	27	P1H.0 / A8
30	P1H.3 / A11	29	P1H.2 / A10
32	P1H.5 / A13 / CC25IO	31	P1H.4 / A12 / CC24IO
34	P1H.7 / A15 / CC27IO	33	P1H.6 / A14 / CC26IO
36	RSTOUT#	35	RSTIN#
38	P6.2 / CS2#	37	NMI#
40	P6.4 / CS4#	39	P6.3 / CS3#
42	P6.6 / HLDA#	41	P6.5 / HOLD#
44	P8.0 / CC16IO	43	P6.7 / BREQ#
46	P8.2 / CC18IO	45	P8.1 / CC17IO
48	P8.4 / CC20IO	47	P8.3 / CC19IO
50	P8.6 / CC22IO	49	P8.5 / CC21IO
52	P7.0 / POUT0	51	P8.7 / CC23IO
54	P7.2 / POUT2	53	P7.1 / POUT1
56	P7.4 / CC28IO	55	P7.3 / POUT3
58	P7.6 / CC30IO	57	P7.5 / CC29IO
60	DGND	59	VCC5V
62	*NC – P9.0*	61	P7.7 / CC31IO
64	*NC - P9.2*	63	*NC - P9.1*
66	*NC - P9.4*	65	*NC - P9.3*
68	*NC - P9.6*	67	*NC - P9.5*
70	*NC – USB*	69	*NC - P9.7*
72	P2.0 / CC0IO	71	*NC - USB*
74	P2.2 / CC2IO	73	P2.1 / CC1IO
76	P2.4 / CC4IO	75	P2.3 / CC3IO
78	P2.6 / CC6IO	77	P2.5 / CC5IO
80	P2.8 / CC8IO / EX0IN	79	P2.7 / CC7IO
82	P2.10 / CC10IO / EX2IN	81	P2.9 / CC9IO / EX1IN
84	P2.12 / CC12IO / EX4IN	83	P2.11 / CC11IO / EX3IN
86	P2.14 / CC14IO / EX6IN	85	P2.13 / CC13IO / EX5IN
88	*NC - IOM2*	87	P2.15 / CC15IO / EX7IN / T7IN
90	*NC - IOM2*	89	*NC - IOM2*
92	*NC - IOM2*	91	*NC - IOM2*
94	*NC – JTAG*	93	*NC - JTAG*
96	*NC – JTAG*	95	*NC - JTAG*
98	*NC – JTAG*	97	*NC - JTAG*
100	*NC – JTAG*	99	*NC - JTAG*
102	P5.1 / AN1	101	P5.0 / AN0
104	P5.3 / AN3	103	P5.2 / AN2
106	P5.5 / AN5	105	P5.4 / AN4
108	P5.7 / AN7	107	P5.6 / AN6
110	P5.9 / AN9	109	P5.8 / AN8
112	P5.11 / AN11 / T5EUD	111	P5.10 / AN10 / T6EUD
114	P5.13 / AN13 / T5IN	113	P5.12 / AN12 / T6IN
116	P5.15 / AN15 / T2EUD	115	P5.14 / AN14 / T4EUD
118	AGND	117	VAREF
120	DGND	119	VCC5V

***NC – xxx* is not connected / for future use**



Pin No X1	Function	Pin No X1	Function
2	DGND	1	VCC5V
4	RTS#	3	DTR#
6	OUT2#	5	OUT1#
8	CD#	7	RI#
10	CTS#	9	DSR#
12	*NC - Uart_opt*	11	BAUDOUT#
14	TxD1	13	RxD1
16	XR12	15	XR13
18	P0H.6 / AD14	17	P0H.7 / AD15
20	P0H.4 / AD12	19	P0H.5 / AD13
22	P0H.2 / AD10	21	P0H.3 / AD11
24	P0H.0 / AD8	23	P0H.1 / AD9
26	P0L.6 / AD6	25	P0L.7 / AD7
28	P0L.4 / AD4	27	P0L.5 / AD5
30	P0L.2 / AD2	29	P0L.3 / AD3
32	P0L.0 / AD0	31	P0L.1 / AD1
34	ALE	33	EA#
36	WRLB#	35	READY#
38	P4.7 / A23 / CAN2_TxD[167CS]	37	RD#
40	DGND	39	VCC5V
42	P4.5 / A21 / CAN1_RxD[167CR]	41	P4.6 / A22 / CAN1_TxD[167CR]
44	P4.3 / A19	43	P4.4 / A20 / CAN2_RxD[167CS]
46	P4.1/A17	45	P4.2/A18
48	*NC – reserved*	47	P4.0/A16
50	VPP	49	*NC – Reserved*
52	RSINS#	51	VBAT
54	LOWL#	53	BOOTSTR#
56	RxD0#	55	TxD0#
58	RxD1#	57	TxD1#
60	CAN1_H	59	CAN2_H
62	CAN1_L	61	CAN2_L
64	*NC - P3.14*	63	P3.15 / CLKOUT / FOUT
66	P3.12/WRHB#	65	P3.13 / SCLK
68	P3.10 / TxD0	67	P3.11 / RxD0
70	P3.8 / MRST	69	P3.9 / MTSR
72	P3.6 / T3IN	71	P3.7 / T2IN
74	P3.4 / T3EUD	73	P3.5 / T4IN
76	P3.2 / CAPIN	75	P3.3 / T3OUT
78	P3.0 / T0IN	77	P3.1 / T6OUT
80	DGND	79	VCC5V

9.1 Mechanikal Drawing



10 Order Code TQM167U:

Module	Order Code	Description
TQM167UK7RCS032	TQM167U-AB	Module TQM167U with • SAB-C167CS Processor • 20 MHz Processor Speed • 1MByte Flash Bottom Boot, 70ns • 1 MByte SRAM, 50ns • with RS232 Driver • with external UART • with CAN driver 1 and CAN driver 2 • with 7 segment display • temperature range 0°C..70°C
TQM167UK7KCR16	TQM167U-AC	Module TQM167U with • SAB-C167CR Processor • 20 MHz Processor Speed • 1MByte Flash Bottom Boot, 70ns • 1 MByte SRAM, 70ns • with RS232 Driver • with external UART • with CAN driver 1 • temperature range 0°C..70°C
TQM167UK7KCR24	TQM167U-AF	Module TQM167U with • SAB-C167CR Processor • 20 MHz Processor Speed • 1MByte Flash Bottom Boot, 70ns • 1 MByte SRAM, 70ns • with RS232 Driver • with external UART • temperature range 0°C..70°C

TQM *v_1* **U** *w_1 w_2 x v_2 s z t*

t: Temperature Range

blank	=	0°C...+70°C
I	=	-40°C...+85°C

sz: Options

Basic Options

blank	=	Standard (RS232, UART, EEPROM, CAN Driver)
001	=	without RS232 Driver
002	=	without external UART
004	=	without EEPROM
008	=	without CAN Driver 1
016	=	without CAN Driver 2
032	=	with 7 Segment Display

s: CPU Clock Speed

blank	=	20 MHz
A	=	24 MHz

v_2: Microcontroller Version

CR	=	Infineon C167CR
CS	=	Infineon C167CS

x: SRAM Memory

A	=	256 kByte (2* 128 kBit * 8 / 1 Mbit), 70 ns
C	=	1 MByte (2* 512 kBit * 8 / 4 Mbit), 70 ns
D	=	2 MByte (2* 1 MBit * 8 / 8 Mbit), 70 ns
H		256 kByte (2* 128 kBit * 8 / 1 Mbit), 55 ns
K	=	1 MByte (2* 512 kBit * 8 / 4 Mbit), 55 ns
L	=	2 MByte (2* 1 MBit * 8 / 8 Mbit), 55 ns
P	=	256 kByte (2* 128 kBit * 8 / 1 Mbit), 50 ns
R	=	1 MByte (2* 512 kBit * 8 / 4 Mbit), 50 ns
S	=	2 MByte (2* 1 MBit * 8 / 8 Mbit), 50 ns

w: Flash Memory

W_2: Speed Option

9	=	90 ns
7	=	70 ns
5	=	55 ns

w_1: Flash Memory Type

A	=	256 kByte (128 kBit * 16 / 2 Mbit), Top Boot
B	=	512 kByte (256 kBit * 16 / 4 Mbit), Top Boot
C	=	1 MByte (512 kBit * 16 / 8 Mbit), Top Boot
D	=	2 MByte (1 Mbit * 16 / 16 Mbit), Top Boot
H	=	256 kByte (128 kBit * 16 / 2 Mbit), Bottom Boot
I	=	512 kByte (256 kBit * 16 / 4 Mbit), Bottom Boot
K	=	1 MByte (512 kBit * 16 / 8 Mbit), Bottom Boot
L	=	2 MByte (1 Mbit * 16 / 16 Mbit), Bottom Boot

v_1: Microcontroller Version

167	=	Infineon SAB-C167x
S10	=	ST ST10x

11 References

SAB-C167CR / SAB-C167CS Microcontroller

http://www.infineon.com/products/index.htm
Microcontrollers
C167CR Users Manual / C167CS Users Manual

AM29F160DT Flash EPROM

http://www.amd.com/products/products.html
Non Volatile Memory
Flash – 5V only Flash Memory

MAX3233 RS232 Driver

http://www.maxim-ic.com
Products / Data Sheets
Data Sheet MAX3232

KM688100LT-7L / KM684000CLG-5L SRAM

http://www.usa.samsungsemi.com

EXAR ST16C550

http://www.exar.com

Rev No.	Designed by:	Date	Approved by:	Date:	Changes:
001	KOZ	09.12.99			1st Version – preliminary
003	KOZ	09.01.00			3rd Version – preliminary (Layout)
004	KOZ	24.05.00			4th Version – preliminary (XREG / Order Code)
100	KOZ	08.08.00			5th Version – Release and new Order Code
101	ANW	07.02.02		11.02.02	Update mechanical data, Pin assignment revised
102	ANW	25.02.02		25.02.02	Update 7 segment display, Pin assignment revised
103	ANW	01.03.02		01.03.02	Supply voltage range revised